REMARKS

Claims 1-9, 11-19, 21, 24-26, 29, 30, and 34-36 are pending in the present application and were examined. Claims 1-9, 11-19, 21, 24-26, 29, 30, and 34-36 are rejected. The specification and drawings are objected to by the Examiner. In response, Claims 1, 3, 11, 21, 24, 25, 26, and 29 are amended, no claims are cancelled and no claims are added. Applicant respectfully requests reconsideration of pending Claims 1-9, 11-19, 21, 24-26, 29, 30, and 34-36 in view of at least the following remarks.

I. Objections to the Claims

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. In response, Claims 24 and 29 are amended to depend from Claims 21 and 26, respectively. In addition, Claim 24 is amended to refer to the partitioning of the sequential application program and to the plurality of program threads of Claim 21.

Regarding Claim 2, Claim 2 is amended to indicate that the status of the Claim is "original."

Claims 11 and 35 are objected to because of informalities. In response, Claims 11, and 35 are amended to replace reference to bonding instructions with "boundary instructions" to provide antecedent basis for such boundary instructions. In addition, Claims 35 and 36 are amended as suggested by the Examiner. In view of Applicant's amendments to Claims 2, 11, 24, 29 and 35, Applicants respectfully request that the Examiner withdraw the objection to Claims 2, 11, 24, 29, and 35-36.

II. Claim Rejections Under 35 U.S.C. §112

Claims 24-25 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention.

In response, Claim 24 is amended to recite the following features:

receiving an indication of the identified critical sections within the sequential application program;

generating the plurality of application program threads according to the thread count to synchronize access to the identified critical sections among the thread program loops; and

processing the identified critical sections to reduce an amount of code contained within the critical sections of the thread program loops.

In view of Applicant's amendments to the above claims, Applicants respectfully submit that Claims 24-25 particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Consequently, in view of such amendments to Claim 24, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §112, second paragraph rejection of Claims 24-25.

V. Claim Rejections Under 35 U.S.C. §103

Claims 1-2, 11-12, 21, 24, 26, 29, and 34-35 are rejected under 35 U.S.C. §103(a) as being anticipated by Sohi et al, ("Multiscalar Processors", 1995, ACM 0-89791-698; pp. 414-425) ("Sohi"). Applicants respectfully disagree with the Examiner's assertions and characterizations of the cited reference, and therefore traverse this rejection of Claims 1-2, 11-12, 21, 24, 26, 29, and 34-35.

Claim 1 recites:

2. A method comprising:

building a control flow graph (CFG) for a loop body of a sequential application program to form a CFG loop;

updating nodes of the CFG loop to enclose identified critical sections of the sequential application program within corresponding pairs of boundary instructions; and

modifying the updated nodes of the CFG loop reduce an amount of instructions between the corresponding pairs of boundary instructions to form a modified CFG loop;

concurrently executing a plurality of application program thread partitions that are generated from the modified CFG loop ; and

synchronizing execution of the identified critical sections of the sequential application program among the plurality of concurrently executing application program threads to ensure that the identified critical sections are executed in a sequential thread order. (Emphasis added.)

Sohi is generally directed to multi-scalar processors and describes the philosophy of the multi-scalar paradigm, the structure of multi-scalar programs, and the hardware architecture of a

multi-scalar processor. In contrast with Claim 1, Sohi does not disclose or suggest modifying the updated nodes of the CFG loop to reduce an amount of instruction between corresponding pairs of boundary instructions to form a modified CFG loop, much less concurrently executing a plurality of application program threads that are generated from the modified CFG loop, as in Claim 1. Sohi does disclose establishment of a large and accurate dynamic window of instructions from which independent instructions can be extracted and scheduled for parallel execution (see page 415, first paragraph under section 2.1), however, that is something completely different from modifying the updated nodes of the CFG loop to reduce an amount of instructions between corresponding pairs of boundary instructions to form a modified CFG loop, much less concurrently executing a plurality of application program threads that are generated from the modified CFG loop, as in Claim 1.

Furthermore, in contrast with Claim 1, Sohi does not disclose or suggest synchronizing execution of the identified critical sections of the sequential application program among the plurality of the concurrently executing application program threads to ensure that the identified critical sections are executed in a sequential thread order, as in Claim1. (See Applicant's specification, pg. 8, para. 0043.) The Examiner has not identified and Applicants are unable to discern any disclosure, teaching, or suggestion regarding synchronizing execution of the identified critical sections of the concurrently executing application program threads to ensure that the identified critical sections are executed in sequential thread order, as in Claim 1. We submit that neither sections 2.1, 2.2, nor any other disclosure of Sohi teaches or suggests synchronizing execution of the identified critical sections of the sequential application program among the plurality of the concurrently executing application program threads to ensure that the identified critical sections are executed in a sequential thread order, as in Claim 1.

For each of the above reasons, Claim 1, and all claims which depend from Claim 1, are patentable over the cited art. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 1 and 2.

Each of Applicants' other independent claims includes features similar to those highlighted above in Claim 1. Therefore, all of Applicants' other independent claims, and all claims which depend on them, are also patentable over the cited art, for similar reasons.

Consequently, we request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 11-12, 21, 24, 26, 29, and 34-35.

Claims 3-9, 13-19, 25, 30, and 36 are rejected under 35 U.S.C. 103(a) as being Sohi in view of Vijaykumar T.N., ("Compiling for the Multiscalar Architecture", University of Wisconsin, 1998, pp. 1-191) "(Vijaykumar"). Applicants respectfully disagree with the Examiner's assertions and characterizations of the cited reference, and therefore traverse this rejection.

DEPENDENT CLAIMS

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicant's silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-36, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 2/21/08

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____ 2/21/08
Elaine Kwak Date